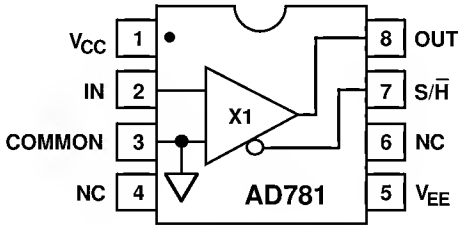
Complete 700 ns Sample-and-Hold Amplifier

AD781*

FEATURES
Acquisition Time to 0.01%: 700 ns Maximum
Low Power Dissipation: 95 mW
Low Droop Rate: 0.01 μV/μs
Fully Specified and Tested Hold Mode Distortion
Total Harmonic Distortion: –80 dB Maximum
Aperture Jitter: 75 ps Maximum
Internal Hold Capacitor
Self-Correcting Architecture
8-Pin Mini Cerdip and Plastic Package
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD781 is a high speed monolithic sample-and-hold amplifier (SHA). The AD781 guarantees a maximum acquisition time of 700 ns to 0.01% over temperature. The AD781 is specified and tested for hold mode total harmonic distortion and hold mode signal-to-noise and distortion. The AD781 is configured as a unity gain amplifier and uses a self-correcting architecture that minimizes hold mode errors and insures accuracy over temperature. The AD781 is self-contained and requires no external components or adjustments.

The low power dissipation, 8-pin mini-DIP package and completeness make the AD781 ideal for highly compact board layouts. The AD781 will acquire a full-scale input in less than 700 ns and retain the held value with a droop rate of 0.01 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD781 ideal for 12- and 14-bit high speed analog-to-digital converters.

The AD781 is manufactured on Analog Devices' BiMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The AD781 is specified for three temperature ranges. The J grade device is specified for operation from 0°C to +70°C, the A grade from –40°C to +85°C and the S grade from –55°C to +125°C. The J and A grades are available in 8-pin plastic DIP packages. The S grade is available in an 8-pin cerdip package.

***Protected by U.S. Patent No. 4,962,325.**

PRODUCT HIGHLIGHTS

1. Fast acquisition time (700 ns), low aperture jitter (75 ps) and fully specified hold mode distortion make the AD781 an ideal SHA for sampling systems.
2. Low droop (0.01 μV/μs) and internally compensated hold mode error results in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD781 an ideal choice for a variety of high performance, low power applications.
4. The AD781 requires no external components or adjustments.
5. Excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.
7. The AD781 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD781/883B data sheet for detailed specifications.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD781–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 10%, V_{EE} = –12 V ± 10%, C_L = 20 pF, unless otherwise noted)

Parameter	AD781J Min	AD781J Typ	AD781J Max	AD781A Min	AD781A Typ	AD781A Max	AD781S Min	AD781S Typ	AD781S Max	Units
SAMPLING CHARACTERISTICS										
Acquisition Time										
10 V Step to 0.01%		600	700		600	700		600	700	ns
10 V Step to 0.1%		500	600		500	600		500	600	ns
Small Signal Bandwidth		4			4			4		MHz
Full Power Bandwidth		1			1			1		MHz
HOLD CHARACTERISTICS										
Effective Aperture Delay (25°C)	**–35**	–25	**–15**	**–35**	–25	**–15**	**–35**	–25	**–15**	ns
Aperture Jitter (25°C)		50	75		50	75		50	75	ps
Hold Settling (to 1 mV, 25°C)		250	**500**		250	**500**		250	**500**	ns
Droop Rate		0.01	**1**		0.01	**1**		0.01	**1**	µV/µs
Feedthrough (25°C)										
(V_{IN} = ±5 V, 100 kHz)		–86			–86			–86		dB
ACCURACY CHARACTERISTICS[1]										
Hold Mode Offset	**–4**	–1	**+3**	**–4**	–1	**+3**	**–4**	–1	**+3**	mV
Hold Mode Offset Drift		10			10			10		µV/°C
Sample Mode Offset		50	**200**		50	**200**		50	**200**	mV
Nonlinearity		±0.002	±0.003		±0.002	±0.003		±0.003	±0.005	% FS
Gain Error		±0.01	**±0.025**		±0.01	**±0.025**		±0.01	**±0.025**	% FS
OUTPUT CHARACTERISTICS										
Output Drive Current	**–5**		**+5**	**–5**		**+5**	**–5**		**+5**	mA
Output Resistance, DC		0.3	**0.5**		0.3	**0.5**		0.3	**0.5**	Ω
Total Output Noise (DC to 5 MHz)		150			150			150		µV rms
Sampled DC Uncertainty		85			85			85		µV rms
Hold Mode Noise (DC to 5 MHz)		125			125			125		µV rms
Short Circuit Current										
Source		20			20			20		mA
Sink		10			10			10		mA
INPUT CHARACTERISTICS										
Input Voltage Range	–5		+5	–5		+5	–5		+5	V
Bias Current		50	**250**		50	**250**		50	**250**	nA
Input Impedance		50			50			50		MΩ
Input Capacitance		2			2			2		pF
DIGITAL CHARACTERISTICS										
Input Voltage Low			**0.8**			**0.8**			**0.8**	V
Input Voltage High	**2.0**			**2.0**			**2.0**			V
Input Current High (V_{IN} = 5 V)		2	**10**		2	**10**		2	**10**	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	±10.8	±12	±13.2	±10.8	±12	±13.2	±10.8	±12	±13.2	V
Supply Current		4	**6.5**		4	**6.5**		4	**7**	mA
+PSRR (+12 V ± 10%)	**70**	80		**70**	80		**70**	80		dB
–PSRR (–12 V ± 10%)	**65**	75		**65**	75		**65**	75		dB
Power Consumption		95	175		95	175		95	185	mW
TEMPERATURE RANGE										
Specified Performance	0		+70	–40		+85	–55		+125	°C

NOTE

[1]Specified and tested over an input range of ±5 V.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

HOLD MODE AC SPECIFICATIONS

(T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 10%, V_{EE} = -12 V ± 10%, C_L = 20 pF, unless otherwise noted)[1]

Parameter	AD781J Min	AD781J Typ	AD781J Max	AD781A Min	AD781A Typ	AD781A Max	AD781S Min	AD781S Typ	AD781S Max	Units
TOTAL HARMONIC DISTORTION										
F_{IN} = 10 kHz		–90	**–80**		–90	**–80**		–90	**–80**	dB
F_{IN} = 50 kHz		–73			–73			–73		dB
F_{IN} = 100 kHz		–68			–68			–68		dB
SIGNAL-TO-NOISE AND DISTORTION										
F_{IN} = 10 kHz	**72**	78		**72**	78		**72**	78		dB
F_{IN} = 50 kHz		73			73			73		dB
F_{IN} = 100 kHz		67			67			67		dB
INTERMODULATION DISTORTION										
F_{IN1} = 49 kHz, F_{IN2} = 50 kHz										
2nd Order Products		–77			–77			–77		dB
3rd Order Products		–78			–78			–78		dB

NOTE
[1]F_{IN} amplitude = 0 dB and F_{SAMPLE} = 500 kHz unless otherwise indicated.

Specifications shown in **boldface** are tested on all devices at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested.

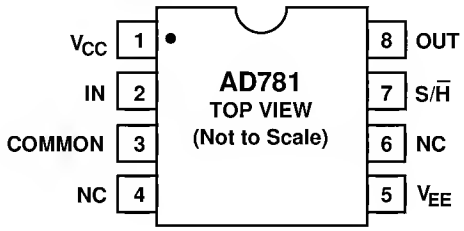
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Unit
V_{CC}	Common	–0.3	+15	V
V_{EE}	Common	–15	+0.3	V
Control Input	Common	–0.5	+7	V
Analog Input	Common	–12	+12	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		–65	+150	°C
Lead Temperature (10 sec max)			+300	°C
Power Dissipation			195	mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

PIN CONFIGURATION



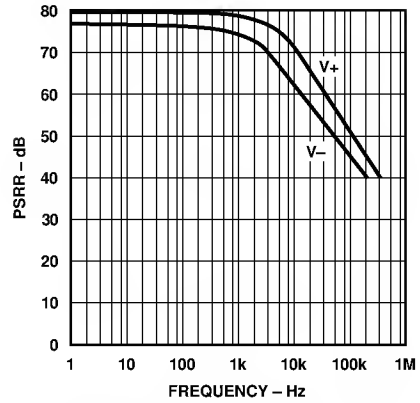
ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Options[2]
AD781JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD781AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD781SQ	–55°C to +125°C	8-Pin Cerdip	Q-8

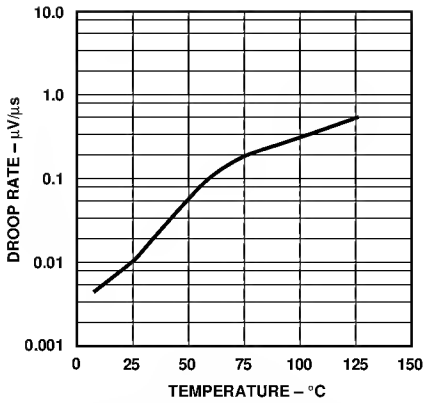
NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD781/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip.

CAUTION

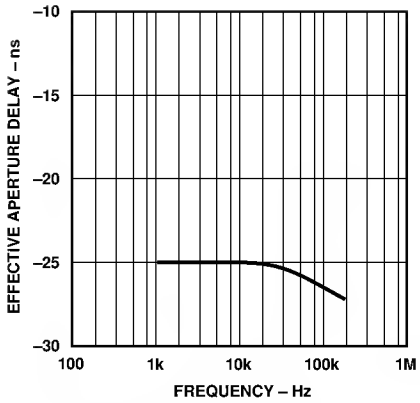
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.



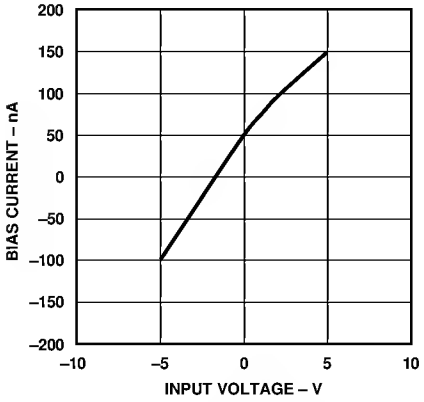
Power Supply Rejection Ratio vs. Frequency



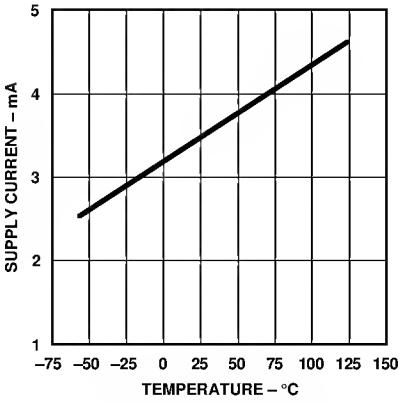
Droop Rate vs. Temperature, V_{IN} = 0 V



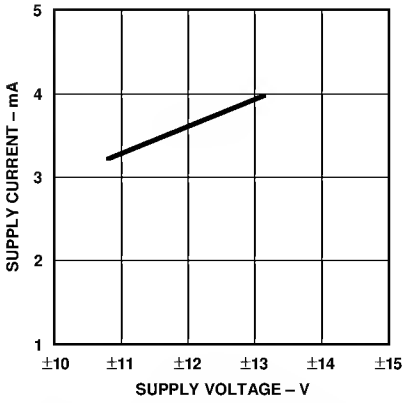
Effective Aperture Delay vs. Frequency



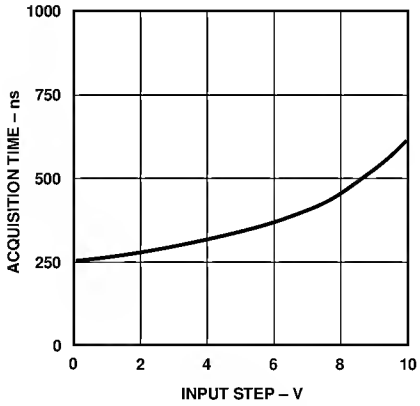
Bias Current vs. Input Voltage



Supply Current vs. Temperature



Supply Current vs. Supply Voltage



Acquisition Time (to 0.01%) vs. Input Step Size

DEFINITIONS OF SPECIFICATIONS

Acquisition Time—The length of time that the SHA must remain in the sample mode in order to acquire a full-scale input step to a given level of accuracy.

Small Signal Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 100 mV p-p sine wave.

Full Power Bandwidth—The frequency at which the held output amplitude is 3 dB below the input amplitude, under an input condition of a 10 V p-p sine wave.

Effective Aperture Delay—The difference between the switch delay and the analog delay of the SHA channel. A negative number indicates that the analog portion of the overall delay is greater than the switch portion. This effective delay represents the point in time, relative to the hold command, that the input signal will be sampled.

Aperture Jitter—The variations in aperture delay for successive samples. Aperture jitter puts an upper limit on the maximum frequency that can be accurately sampled.

Hold Settling Time—The time required for the output to settle to within a specified level of accuracy of its final held value after the hold command has been given.

Droop Rate—The drift in output voltage while in the hold mode.

Feedthrough—The attenuated version of a changing input signal that appears at the output when the SHA is in the hold mode.

Hold Mode Offset—The difference between the input signal and the held output. This offset term applies only in the hold mode and includes the error caused by charge injection and all other internal offsets. It is specified for an input of 0 V.

Tracking Mode Offset—The difference between the input and output signals when the SHA is in the track mode.

Nonlinearity--The deviation from a straight line on a plot of input vs. (held) output as referenced to a straight line drawn between endpoints, over an input range of –5 V and +5 V.

Gain Error—Deviation from a gain of +1 on the transfer function of input vs. held output.

Power Supply Rejection Ratio—A measure of change in the held output voltage for a specified change in the positive or negative supply.

Sampled DC Uncertainty—The internal rms SHA noise that is sampled onto the hold capacitor.

Hold Mode Noise—The rms noise at the output of the SHA while in the hold mode, specified over a given bandwidth.

Total Output Noise—The total rms noise that is seen at the output of the SHA while in the hold mode. It is the rms summation of the sampled dc uncertainty and the hold mode noise.

Output Drive Current—The maximum current the SHA can source (or sink) while maintaining a change in hold mode offset of less than 2.5 mV.

Signal-To-Noise and Distortion (S/N+D) Ratio—S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Total Harmonic Distortion (THD)—THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

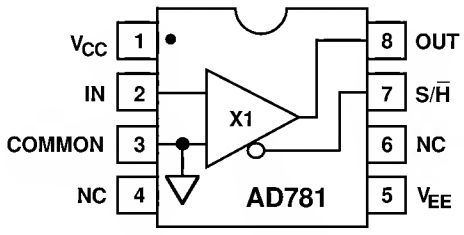
Intermodulation Distortion (IMD)—With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequency of mfa±nfb, where m, n = 0, 1, 2, 3.... Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa+fb) and (fa–fb), and the third order terms are (2fa+fb), (2fa–fb), (fa+2fb) and (fa–2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude, and peak value of their sums is –0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FUNCTIONAL DESCRIPTION

The AD781 is a complete sample-and hold amplifier that provides high speed sampling to 12-bit accuracy in less than 700 ns.

The AD781 is completely self-contained, including an on-chip hold capacitor, and requires no external components or adjustments to perform the sampling function. Both input and output are treated as a single-ended signal, referred to common.

The AD781 utilizes a proprietary circuit design which includes a self-correcting architecture. This sample-and-hold circuit corrects for internal errors after the hold command has been given, by compensating for amplifier gain and offset errors, and charge injection errors. Due to the nature of the design, the SHA output in the sample mode is not intended to provide an accurate representation of the input. However, in hold mode, the internal circuitry is reconfigured to produce an accurately held version of the input signal. Below is a block diagram of the AD781.



Functional Block Diagram

DYNAMIC PERFORMANCE

The AD781 is compatible with 12-bit A-to-D converters in terms of both accuracy and speed. The fast acquisition time, fast hold settling time and good output drive capability allow the AD781 to be used with high speed, high resolution A-to-D converters like the AD674 and AD7672. The AD781's fast acquisition time provides high throughput rates for multichannel data acquisition systems. Typically, the sample and hold can acquire a 10 V step in less than 600 ns. Figure 1 shows the settling accuracy as a function of acquisition time.

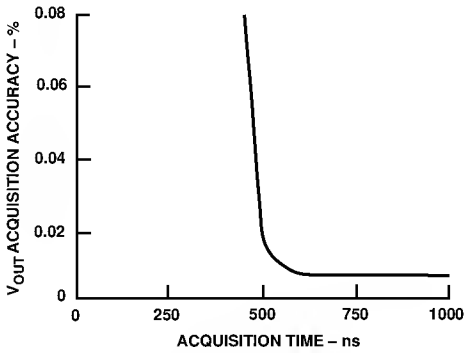


Figure 1. V_{OUT} Settling vs. Acquisition Time

The hold settling determines the required time, after the hold command is given, for the output to settle to its final specified accuracy. The typical settling behavior of the AD781 is shown in Figure 2. The settling time of the AD781 is sufficiently fast to allow the SHA, in most cases, to directly drive an A-to-D converter without the need for an added "start convert" delay.

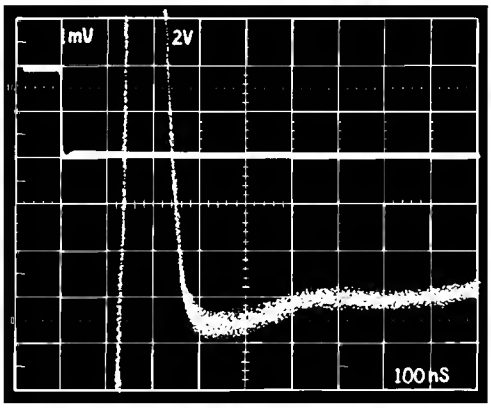


Figure 2. Typical AD781 Hold Mode

HOLD MODE OFFSET

The dc accuracy of the AD781 is determined primarily by the hold mode offset. The hold mode offset refers to the difference between the final held output voltage and the input signal at the time the hold command is given. The hold mode offset arises from a voltage error introduced onto the hold capacitor by charge injection of the internal switches. The nominal hold mode offset is specified for a 0 V input condition. Over the input range of –5 V to +5 V, the AD781 is also characterized for an effective gain error and nonlinearity of the held value, as shown in Figure 3. As indicated by the AD781 specifications, the hold mode offset is very stable over temperature.

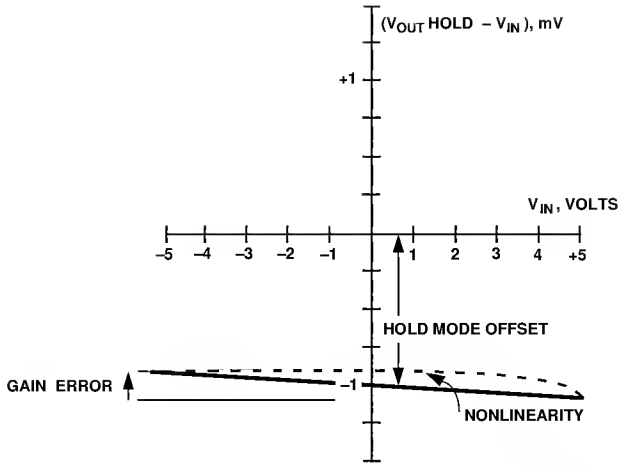


Figure 3. Hold Mode Offset, Gain Error and Nonlinearity

For applications where it is important to obtain zero offset, the hold mode offset may be nulled externally at the input to the A-to-D converter. Adjustment of the offset may be accomplished through the A-to-D itself or by an external amplifier with offset nulling capability (e.g., AD711). The offset will change less than 0.5 mV over the specified temperature range.

SUPPLY DECOUPLING AND GROUNDING CONSIDERATIONS

As with any high speed, high resolution data acquisition system, the power supplies should be well regulated and free from excessive high frequency noise (ripple). The supply connection to the AD781 should also be capable of delivering transient currents to the device. To achieve the specified accuracy and dynamic performance, decoupling capacitors must be placed directly at both the positive and negative supply pins to common. Ceramic type 0.1 μF capacitors should be connected from V_{CC} and V_{EE} to common.

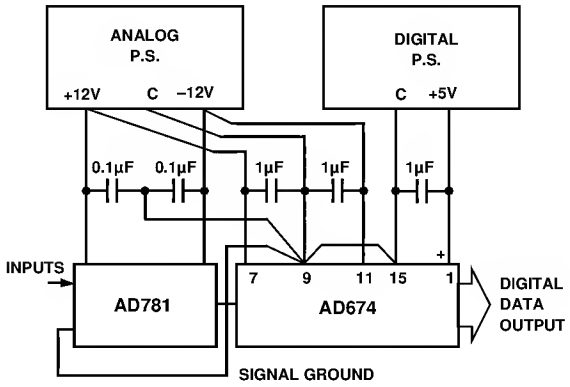


Figure 4. Basic Grounding and Decoupling Diagram

The AD781 does not provide separate analog and digital ground leads as is the case with most A-to-D converters. The common pin is the single ground terminal for the device. It is the reference point for the sampled input voltage and the held output voltage and also the digital ground return path. The common pin should be connected to the reference (analog) ground of the A-to-D converter with a separate ground lead. Since the analog and digital grounds in the AD781 are connected internally, the

common pin should also be connected to the digital ground, which is usually tied to analog common at the A-to-D converter. Figure 4 illustrates the recommended decoupling and grounding practice.

NOISE CHARACTERISTICS

Designers of data conversion circuits must also consider the effect of noise sources on the accuracy of the data acquisition system. A sample-and-hold amplifier that precedes the A-to-D converter introduces some noise and represents another source of uncertainty in the conversion process. The noise from the AD781 is specified as the total output noise, which includes both the sampled wideband noise of the SHA in addition to the band limited output noise. The total output noise is the rms sum of the sampled dc uncertainty and the hold mode noise. A plot of the total output noise vs. the equivalent input bandwidth of the converter being used is given in Figure 5.

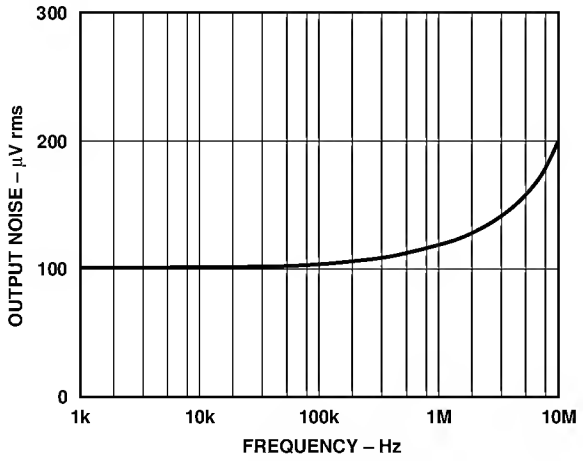


Figure 5. RMS Noise vs. Input Bandwidth of ADC

DRIVING THE ANALOG INPUTS

For best performance, it is important to drive the AD781 analog input from a low impedance signal source. This enhances the sampling accuracy by minimizing the analog and digital crosstalk. Signals which come from higher impedance sources (e.g., over 5 kΩ) will have a relatively higher level of crosstalk. For applications where signals have high source impedance, an operational amplifier buffer in front of the AD781 is required. The AD711 (precision BiFET op amp) is recommended for these applications.

HIGH FREQUENCY SAMPLING

Aperture jitter and distortion are the primary factors which limit frequency domain performance of a sample-and-hold amplifier. Aperture jitter modulates the phase of the hold command and produces an effective noise on the sampled analog input. The magnitude of the jitter induced noise is directly related to the frequency of the input signal.

A graph showing the magnitude of the jitter induced error vs. frequency of the input signal is given in Figure 6.

The accuracy in sampling high frequency signals is also constrained by the distortion and noise created by the sample-and hold. The level of distortion increases with frequency and reduces the "effective number of bits" of the conversion.

Measurements of Figures 7 and 8 were made using a 14-bit A/D converter with V_{IN} = 10 V p-p and a sample frequency of 100 kSPS.

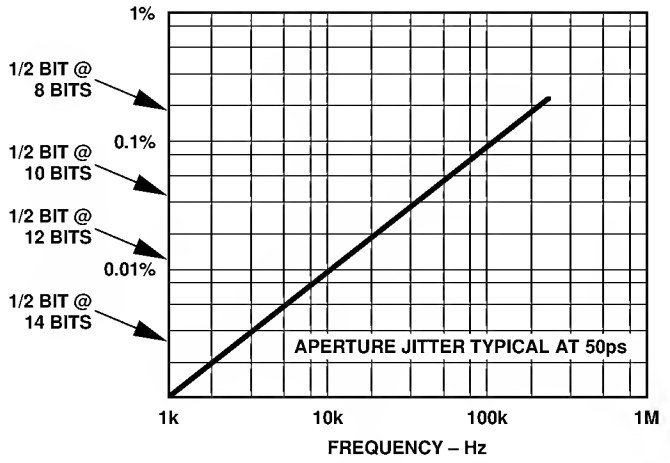


Figure 6. Error Magnitude vs. Frequency

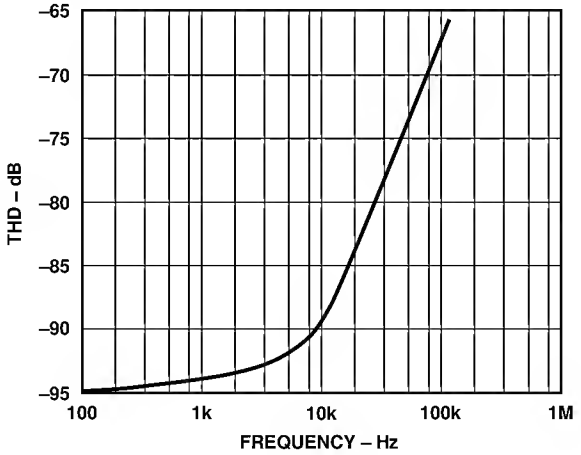


Figure 7. Total Harmonic Distortion vs. Frequency

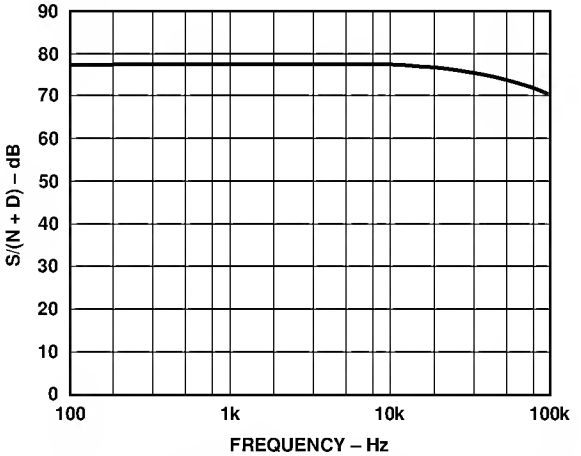


Figure 8. Signal/(Noise and Distortion) vs. Frequency

AD781 TO AD674 INTERFACE

Figure 9 shows a typical data acquisition circuit using the AD781, a high linearity, low aperture jitter SHA and the AD674 a 12-bit high speed ADC. The time between the AD674 status line going high and the actual start of conversion allows the AD781 to settle to 0.01%. As a result, the AD674 status line can be used to control the AD781; only an inverter is needed to interface the two devices.

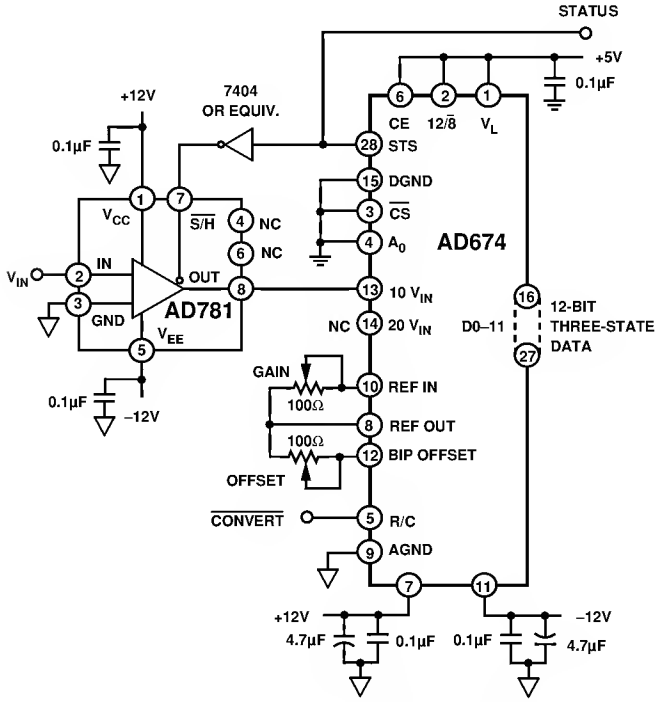


Figure 9. AD781 to AD674 Interface

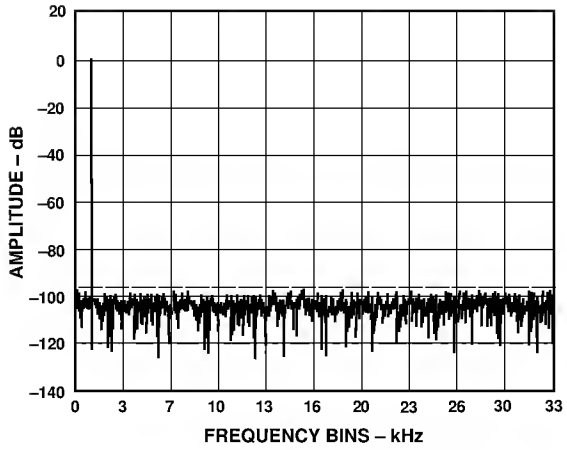


Figure 10. FFT Plot of AD781 to AD674 Interface, F_{IN} = 1 kHz

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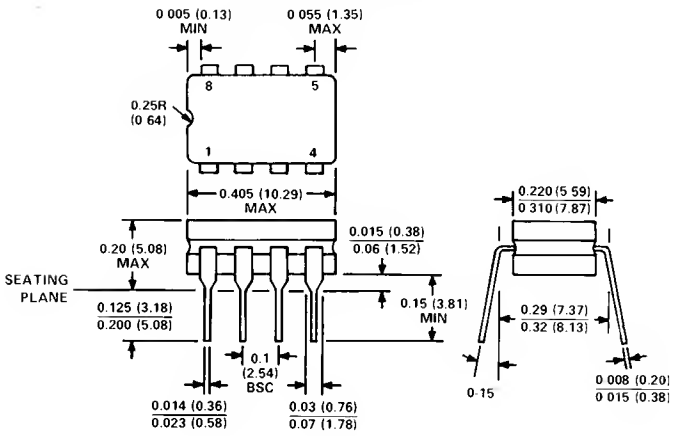
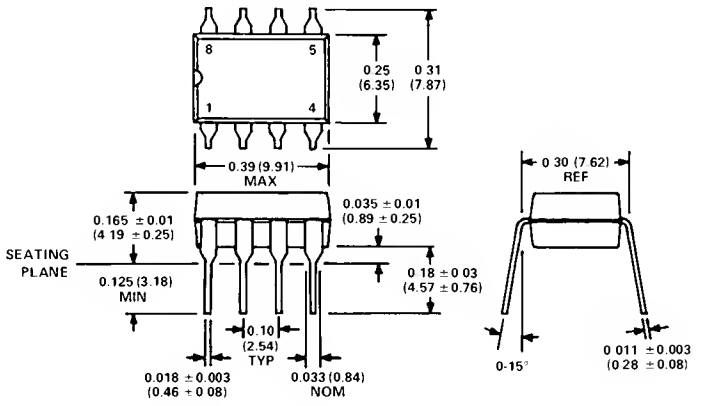
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Cerdip (Q) Package



Mini-DIP (N) Package



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